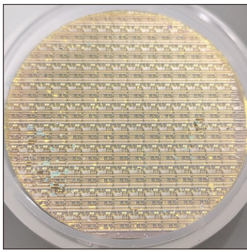

Diamond Wafer for High-Frequency Semiconductor Devices

Yoshiki NISHIBAYASHI*, Yutaka KOBAYASHI, Naoteru SHIGEKAWA, and Jianbo LIANG

With the increasing amount of information handled in high-frequency devices used in wireless communications for base stations, heat generation has become an issue, and there is a demand for device structures with improved heat dissipation. Using diamond, which has high thermal conductivity, as an effective heat sink material has been considered a promising approach. However, with conventional bonding methods, the thermal resistance between the device and the heat sink, which is on the order of several micrometers, is no longer negligible. As a more efficient heat dissipation method, we have succeeded in fabricating a large-diameter GaN-on-polycrystalline diamond structure with a 2-inch diameter, in which a GaN semiconductor device and a diamond heat sink are directly bonded without adhesives or soldering materials. Additionally, we have fabricated a prototype GaN-HEMT device and confirmed its superior heat dissipation characteristics.

Keywords: high heat dissipation, 2-inch diameter, polycrystalline diamond wafer, GaN-HEMT, direct Bonding

1. Introduction

High-frequency devices for fifth-generation and sixth-generation wireless base station communication and semiconductor devices for data centers in recent years must handle ever-increasing amounts of information, so they are required to increase the frequency and current capacity. Under these circumstances, the temperature of semiconductor devices during operation rises, preventing such devices from fully demonstrating their performance. To maximize performance, it is effective to bond a semiconductor chip on diamond, which is a high-heat-dissipating heat spreader, to reduce the temperature rise of the chip. However, the extent of heat dissipation is limited due to thermal resistance caused by the thickness of the semiconductor chip and the solder material used for bonding. To address this issue, a technology has been developed to further improve the heat dissipation efficiency by using only the active layer, which is a thin film of micrometer order, of semiconductor devices and performing direct bonding*1 to diamond without using a bonding material (device-first process).[1] Meanwhile, a method of directly bonding a semiconductor thin film layer to diamond and then fabricating devices on the semiconductor layer (bonding-first process) is also promising and more suitable for mass production than the former method. In the initial stage of this research and development (R&D) project, direct bonding and device fabrication were verified using a 10-mm-square size,[2] and the high heat dissipation properties of the devices were also confirmed.[3] To scale the technology to mass production, it is essential to conduct evaluations using large-diameter wafers, which are required for semiconductor processing. That is, it is necessary to verify the structure derived from direct bonding of a large-diameter diamond wafer and a semiconductor layer and fabrication of prototype semiconductor devices and to confirm the device operation and high-heat-dissipation properties.

Our report on this R&D project focuses on the development of a large-diameter, 2-inch diamond wafer, on which semiconductor processing can be fully tested at research institutions. It also presents the prototype fabrication of GaN-HEMT*2 devices, which are derived from direct bonding of a wafer and a GaN semiconductor layer,*3 which have been put into practical use for wireless communication, and successful confirmation of the high-heat-dissipation properties.

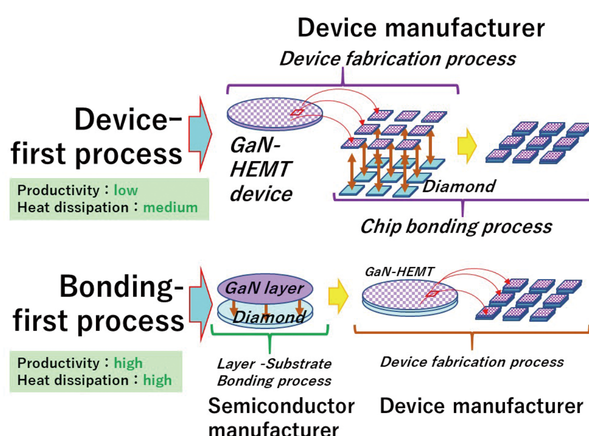

Fig. 1. Fabrication process of the semiconductor-diamond bonded structure

2. Types of Polycrystalline Diamond Wafers

Since the launch of the development of diamond synthesis technology based on chemical vapor deposition in 1983, we have commercialized 10-mm- to 20-mm-square diamond heat sinks and tape automated bonding (TAB) tools*4 in which diamond is laminated on ceramics.[4] Furthermore, the development of large-diameter, 2-inch diamond wafers also started in 1993, which led to commercialization of diamond surface acoustic wave (SAW) filters in 1999.[5], [6] Although the fundamental technology for polycrystalline diamond synthesis has been well estab-

lished, this was the first attempt to develop a large-diameter, 2-inch wafer of laminated polycrystalline diamond with high-heat-dissipation properties.

We have developed various types of free-standing wafer and stacking wafer, as shown in Table 1, using polycrystalline diamond, and their specifications also vary case to case depending on the purpose. In this paper, substrates refer to those with a diameter of less than two inches, and wafers refer to those with a diameter of two inches or more. This was the world's first attempt to directly bond a 2-inch polycrystalline diamond wafer with superior heat dissipation properties to a GaN semiconductor from among various substrates and wafers listed in Table 1. Regarding this application, high-heat-dissipation wafers are (1), (2), (5), and (7) in the "Type" column of Table 1 in terms of the structure. These structures have been used for heat sinks of small sizes measuring 10 mm by 10 mm or less.

With the supply of semiconductor wafers taken into account as one of the key considerations, technology development is underway based on the policy to develop a process with short processing time, achieve a low-cost wafer structure, and further increase the diameter. The structures of (1) and (5) in Table 1 meet the requirements.

Table 1. Diamond substrate / wafer types

	Diamond synthesis method	Diamond grain size of layer	Diamond thickness (μm)	Underlying Substrate	Diamond thermal conductivity (W/mK)	Overall heat dissipation	Cost	Substrate / wafer maximum size in previous SEI R&D	Type
Diamond free-standing sub. / wafer	HFCVD	Coarse (> 10 μm)	> 300	–	> 1000	Excellent	Medium	25×25 mm	(1)
	MPCVD	Coarse (> 10 μm)	> 500	–	> 1800	Excellent	High	2 inch φ	(2)
Diamond stacking sub. / wafer	HFCVD	Fine (< 1 μm)	< 30	Si	< 1000	Low	Low	3 inch φ	(3)
	HFCVD	Coarse (> 10 μm)	< 50	Si	> 1000	Good	Low	25×25 mm	(4)
	HFCVD	Coarse (> 10 μm)	< 50	Ceramics (AlN, SiN, SiC)	>1000	Excellent	Low	10×10 mm	(5)
	MPCVD	Coarse (> 10 μm)	< 50	Si	> 1800	Good	Low	2 inch φ	(6)
	MPCVD	Coarse (> 10 μm)	< 50	Ceramics (AlN, SiN, SiC)	> 1800	Excellent	Low	10×10 mm	(7)

Note) HFCVD: Hot filament chemical vapor deposition
MPCVD: Microwave plasma chemical vapor deposition

3. Polycrystalline Diamond Wafer Production Method

The newly developed diamond wafer is produced by forming polycrystalline diamond on a different material, such as silicon and ceramics, using the chemical vapor deposition method (CVD method). Free-standing wafers are produced by removing the different-material substrate, while stacking wafers are formed with diamond just grown on different materials.

3-1 Polycrystalline diamond synthesis method

Diamond was produced using the hot filament CVD method or the microwave plasma CVD method. A schematic diagram is shown in Fig. 2. Polycrystalline diamond was produced based on well-known conditions in terms of methane concentration and substrate temperature to attain a particle size of 10 μm or more. Regarding free-standing wafers, polycrystalline diamond with a thickness of 300 μm or more was grown on a silicon substrate. The diamond surface was polished before removing the silicon substrate. Silicon was then removed by acids. Regarding stacking wafers, diamond with a thickness of 100 μm or less was grown on silicon or ceramics with a thickness 3 mm or less. The stacking wafers were also mirror-finished by planarizing and polishing the diamond surface.

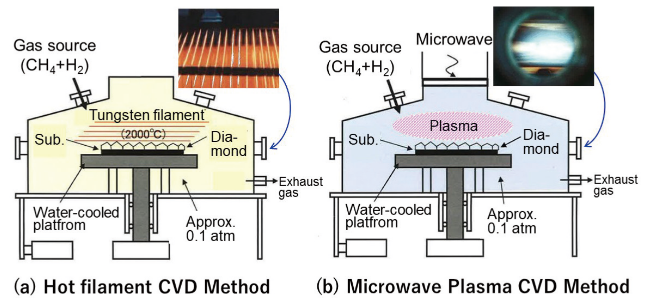

Fig. 2. Schematic diagram of the diamond synthesis system

3-2 Polycrystalline diamond wafer planarization method

In terms of conventional diamond planarization methods, the mainstream approaches are abrasive polishing of a diamond substrate using a polishing wheel with diamond grits and polishing using a cast iron wheel (Scaife). Unlike the semiconductor wafer manufacturing process, a stepwise planarization process comprising the grinding, lapping, and polishing processes was not used. This is because no grinding wheel harder than diamond was available or because no wet chemical polishing methods, including chemically stable CMP,*5 could be applied. It should be noted that cast iron wheels have long been used to polish jewels. When the size is small, measuring 10 mm by 10 mm or less, the surface is planarized by lapping and polishing without significant difficulty. However, when the wafer size is two inches or larger, the polishing speed becomes extremely slow, resulting in a long polishing time. Thus, it is effective to perform stepwise processing of diamond wafers, just like grinding of other semiconductor wafers. In October 2022, we started to develop a laser-based surface trimming technique for rough processing by utilizing a support project of the Japan Science and Technology Agency (JST). This was named partial rough trimming. This was used for pre-processing in the mechanical polishing process. Mechanical

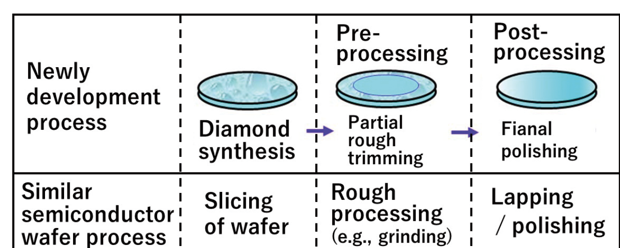

Fig. 3. Diamond wafer planarization process

polishing was performed in the subsequent process in combination with a conventional method using a polishing wheel with diamond grits and a polishing method based on reaction with diamond. Figure 3 shows a schematic diagram of the overall planarization process.

(1) Pre-processing (partial rough trimming)

The amount of diamond processed by polishing (processing depth) can be reduced by performing laser-based trimming before planarization via mechanical polishing. This helps reduce the overall polishing time. Ideally, the processing depth should be the height difference of surface irregularities. The height difference is the polishing depth by precisely aligning the polishing wheel surface with the wafer surface. (Refer to the side view in the lower panel of Fig. 4.)

In laser-based processing, short high-energy laser pulses are irradiated to ablate the diamond surface in an instant. A given volume of diamond is ablated from the surface for processing. The volume of diamond ablated from the surface can be changed by changing the pulse energy, pulse repetition rate, and laser scanning speed, making it possible to control the processing speed. The laser irradiation point can be controlled by a galvanometer mirror. Thus, if two-dimensional irregularity data is available, the height difference can be reduced compared to that before laser processing by irradiating only protrusions with a laser. We confirmed that processing of several μm to 30 μm can be performed per scan by adjusting the aforementioned laser conditions and that the processing depth can be increased in proportion to the number of scans.

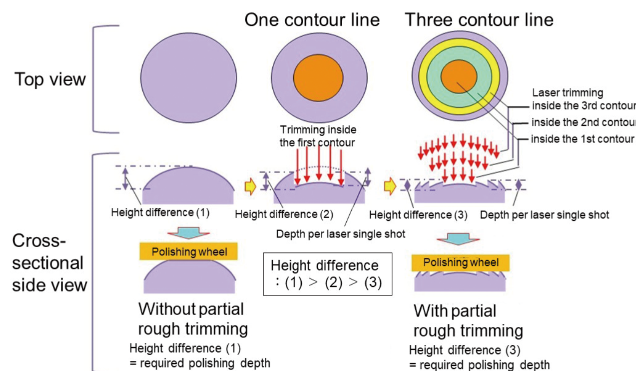

Fig. 4. Illustrated image of partial rough trimming of diamond surface

To remove the height difference more smoothly, contour lines for smaller surface steps should be generated based on the surface irregularity data, and the areas inside the contour lines should be planarized by performing laser processing for the number of surface steps, with the surface steps modeled as a pyramid for simplicity (Fig. 4). The smaller the height difference is, the shorter the time required for polishing is in post-processing.

Diamond was experimentally synthesized on a 2-inch ceramic wafer substrate, and the surface geometry was measured using the Dyvoce (DY-3001YM), manufactured by Kohzu Precision Co., Ltd. The result is shown in the left panel of Fig. 5 (b). A surface height difference (based on the root mean square surface) of 20.6 μm was measured. A contour line was generated to create a surface step of 5 μm from the top, based on the surface irregularity height data, and the area inside the contour line was divided into two steps to perform laser trimming. The result is shown in the right panel of Fig. 5 (b). It was found that the surface height difference after laser processing was 12.4 μm. Figure 5 (a) shows photos before and after experimental trimming. The result seems to be slightly smaller than that of the designed laser processing per step of 5 μm. However, it was found that the height difference reduction and distribution were almost as expected. The trimming takes approximately 10 minutes to complete.

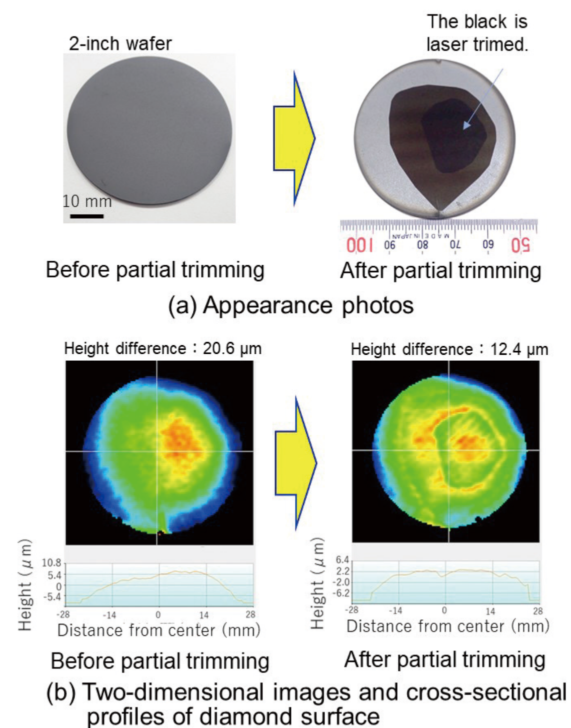

Fig. 5. Example of partial rough trimming of diamond surface

(2) Post-processing (final polishing)

Final polishing is performed through sliding contact between a flat polishing wheel and a wafer. Physical polishing and chemical reaction-assisted polishing can be used. Physical polishing uses a polishing wheel with diamond grits embedded, while chemical reaction-assisted polishing uses cast iron or glass. Because the polishing speed is slow in both approaches, it is essential to minimize the height difference in pre-processing. It is evident from the graph of Fig. 6, which shows the correlation between the height difference and the polishing time, that rough trimming in pre-processing is effective for reducing the polishing time. The polishing time is plotted on the horizontal axis, and the percentage of the polished area relative to the total area is plotted on the vertical axis. When the height difference is 15 μm or less, the polishing time is approximately one sixth that of the height difference of 100 μm.

Photo 1 shows photos of the appearance of the two types of experimentally polished and completed diamond wafers. The photo on the left of Photo 1 has a wafer structure corresponding to (2) in Fig. 1, while the photo on the right has a wafer structure corresponding to (5) in Fig. 1. A fluorescent tube is reflected in the photo to show that the surface is polished to a mirror finish.

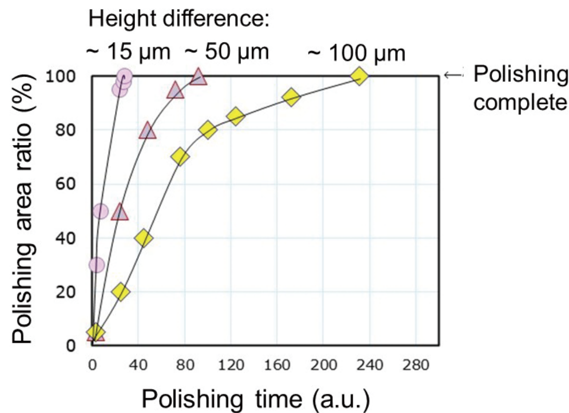

Fig. 6. Correlation between the polishing time and the polishing area ratio

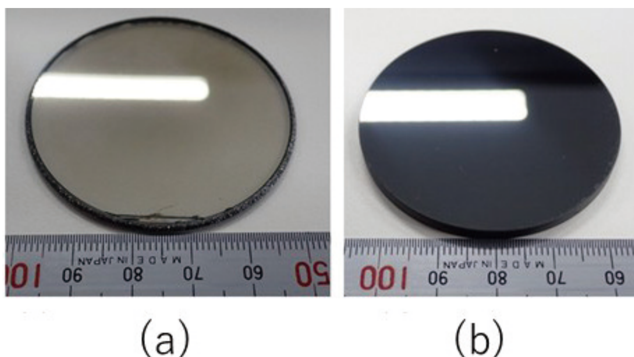

Photo 1. Two types of 2-inch diamond wafers
(a) free-standing wafer and (b) stacking wafer

4. Evaluations of the Polycrystalline Diamond Wafers

The fabricated large-diameter, 2-inch polycrystalline diamond wafers were evaluated for their applicability to high-frequency devices. First, the following points were confirmed based on the bonding-first process: (1) whether a GaN semiconductor layer can be directly bonded to a diamond wafer, (2) whether the GaN-HEMT structure can be fabricated all over the wafer, and (3) whether diamond improves the heat dissipation properties of the GaN-HEMT devices. The details are discussed below.

4-1 Prototype fabrication of GaN-HEMT devices

The process to fabricate GaN-HEMT devices on a 2-inch polycrystalline diamond wafer is as shown in Fig. 7. First, the GaN semiconductor layer was laminated by using direct bonding technology without adhesives or solder materials. Subsequently, the transistor electrodes (source, drain, and gate) were subjected to vapor deposition and photolithography processes to fabricate devices. Figure 8 also shows photos of the overall wafer used for the experiment. Magnified views of the device and cross-sectional structure are as shown in the schematic diagram in Fig. 8. A visual check of the bonding state of the GaN semiconductor layer revealed no particular problems across the entire wafer. Microscopic observation also verified that devices were fabricated across the entire wafer.

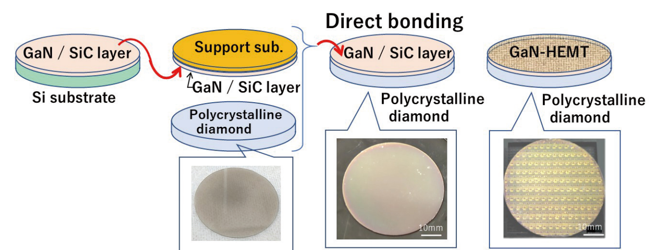

Fig. 7. Fabrication process of GaN-HEMT structure and wafer photos at each process(7)

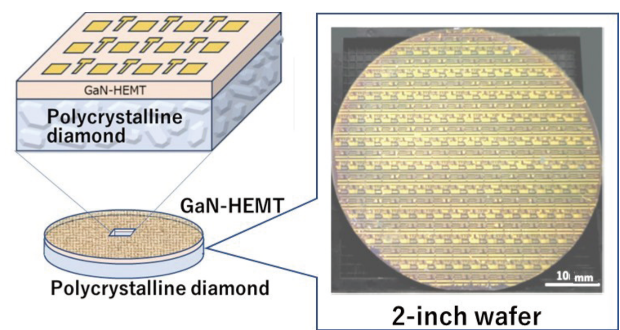

Fig. 8. Schematic diagram of GaN-HEMT structure on a diamond wafer(8)

4-2 Heat dissipation evaluations of GaN-HEMT devices

The bonding state of GaN semiconductor devices on the diamond wafers appears to be sound when observed from the surface. However, the actual bonding state must be confirmed based on whether heat is dissipated properly. The bonding state in the lower part of the devices and nonuniformity on the wafers can be quantitatively evaluated by energizing the respective devices on the wafers and measuring the temperature.

Figure 9 (a) shows a schematic diagram of the GaN HEMT structure and the heat-generating region during device operation. In Fig. 9 (b), applied power is plotted on the horizontal axis to show the temperature rise during operation of GaN HEMT devices fabricated on different types of substrates. Si has the lowest thermal conductivity, followed by SiC, and then diamond, and the temperature rise is reduced accordingly. This shows that diamond has the highest heat-dissipation properties.

We also studied the temperature rise of two-terminal devices fabricated on a 2-inch polycrystalline diamond wafer and a silicon wafer. The results are shown in Fig. 10. The device numbers on each wafer are plotted on the hori-

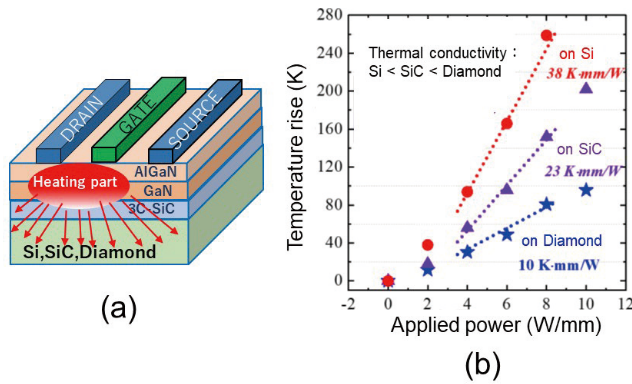

Fig. 9. (a) Transistor structure and heat-generating region, and (b) Temperature rise during device operation on different types of substrate[9] (Heat dissipation: on Si < on SiC < on daimond)

zontal axis. Devices are distributed across the wafer. The vertical axis represents the temperature rise of each device. As in the case of Fig. 9 (b), devices on diamond demonstrated good heat-dissipation properties compared to those on Si. The temperature rise across the wafer surface at the same power was almost uniform (unevenness: up to a few percent). With the precision of the device geometry and consistency of diamond quality taken into account, the bonding state is considered to be highly uniform and satisfactory.[8], [10]

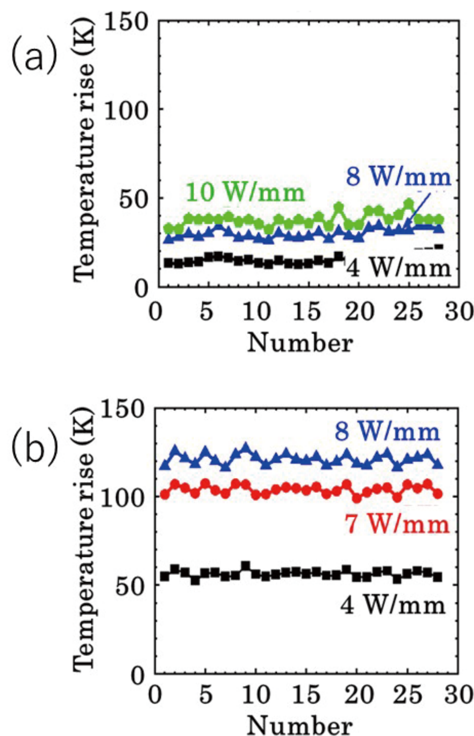

Fig. 10. Temperature rise of each device on wafer (a) on diamond and (b) on Si

5. Conclusion

We were able to fabricate large-diameter, 2-inch diamond wafers with high thermal conductivity of 1,000 W/mK or more. The main polishing process for such fabrication technology was divided into pre-processing and post-processing, and laser-based trimming was adopted for pre-processing to perform rough processing for planarization. The effectiveness of the new process seems to be limited for the 2-inch size. However, we are confident that the process will demonstrate even greater effects for large-diameter sizes of four inches or more, which is our next step. We were able to establish a fabrication process for 4-inch wafers.

Furthermore, we also succeeded in directly bonding the large-diameter, 2-inch polycrystalline wafer to a GaN semiconductor for high-frequency devices, which is the objective of the paper. In addition to confirmation of bonding based on a visual check and microscopic observation, we confirmed that the bonding ensures physical adhesion effective for heat dissipation based on prototype device fabrication and temperature rise during operation. While previous research projects verified applicability to a size of approximately 10 mm by 10 mm, our results show applicability to large-diameter wafers. The achievement will lead to a manufacturing process for mass production.

There are still challenges to be overcome. It is necessary to ensure deployment to 4-inch diamond wafers and GaN-on-diamond wafers, achieve specifications suitable for the manufacturing equipment for semiconductor processing, which is currently used for wafers with this structure, and realizing the process up to chip production at low cost. While addressing these challenges, we hope that this technology will be widely applied as a heat dissipation solution for semiconductor devices beyond the application to high-frequency devices.

6. Acknowledgments

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Technical Terms

*1 Direct bonding: This method enables direct bonding of substrate materials without using adhesive materials, such as solder. The technology forms a clean, highly activated state on both substrate surfaces to be bonded and achieves atomic bonding by simply bringing both surfaces into close contact.

*2 HEMT: Abbreviation for “High Electron Mobility Transistor.” The transistor is derived from epitaxial growth of a semiconductor with a greater energy gap on the semiconductor layer and achieves high electron mobility due to quantum states at the bonding interface. It refers to a transistor structure commonly used in compound semiconductors.

*3 GaN semiconductor layer: A thin film layer of a wide bandgap compound semiconductor named gallium nitride. The semiconductor is applied to blue light-emitting diodes (LEDs) and high-frequency transistors.

*4 TAB tool: One of the packaging technologies widely used to mount integrated circuits (ICs) on liquid crystal displays (LCDs). It refers to a soldering tool used to connect electrodes and wires.

*5 CMP: Abbreviation for "Chemical Mechanical Polish." It refers to mirror finishing for final polishing of semiconductor wafers.

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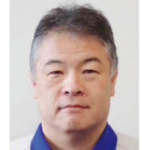

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