SiC High Blocking Voltage Transistor

Ren KIMURA*, Kousuke UCHIDA, Toru HIYOSHI, Mitsuhiko SAKAI, Keiji WADA
and Yasuki MIKAMURA

Recently, with the growing global interest in energy saving, power device efficiency is increasingly important. Most power devices are fabricated utilizing silicon (Si) and the performance of Si has reached its limit. Silicon Carbide (SiC) is the best candidate material for innovative power devices that can replace Si devices. The authors have developed SiC Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) with high blocking voltage and low specific on-resistance characteristics that take full advantage of SiC. This paper provides an overview of the design, fabricating process, and electrical properties of high blocking voltage SiC MOSFETs. The edge termination technique is applied to SiC MOFSETs, shows a high blocking voltage of 3,850 V, and a low specific on-resistance of 14.2 mΩ cm^2. These results show that the application of SiC to power electronics will provide significant benefits in improving efficiency with high voltage operation.

Keywords: silicon carbide, blocking voltage, transistor, power device

1. Introduction

Recently, energy saving is strongly required to prevent global warming. Electricity is the most common energy form and is necessary in our daily life and various activities, because it is comparatively easy to utilize in transmission and conversion after generation. Therefore, it is very important to reduce energy loss in electric power systems and improve their efficiency. The present power systems basically consist of semiconductor power devices made of silicon (Si). Though the devices have been developed by structural modification with advanced microfabrication, it is impossible to overcome the material limits of Si. Therefore, it is strongly expected to develop alternative power devices that exceed the material limits of Si.

Silicon Carbide (SiC) has become a candidate material for next generation power devices to replace traditional Si power devices. Among the various crystalline polytypes of SiC, 4H-SiC is the most promising as a semiconductor material for power devices. In comparison to Si, 4H-SiC has several advantages, such as wide bandgap, high breakdown field, high thermal conductivity, and high saturation velocity. As the critical breakdown field of 4H-SiC is about three times higher than that of Si, SiC devices can be superior power devices in the category of higher voltage applications. Under conditions for keeping a certain blocking voltage, thickness of the drift region for SiC is one tenth of that for Si. Also, doping concentration is a hundred times higher than that of Si. As these give an advantage in decreasing resistance in the drift layer, a specific on-resistance of SiC is estimated to be two or three orders of magnitude less than that of Si.

On the other hand, as the saturation drift velocity of 4H-SiC is twice higher than that of Si, 4H-SiC is also expected to be a better material for high speed switching applications.

As thermal conductivity of 4H-SiC is three times higher than that of Si, 4H-SiC devices can be utilized under a simple cooling system.

In the present application of high voltage inverters and converters for industrial motors, the Si Insulated Gate Bipolar Transistors (IGBTs) with a blocking voltage of 1,200-3,300 V are generally adopted. However, due to the advantages of 4H-SiC devices described above, SiC MOSFET are expected to replace Si IGBT.

In this paper, the authors report on the SiC MOSFET with a blocking voltage of 2,200 V and 3,300 V and its characteristics. The device design and the fabrication processes are also discussed.

2. Device Design and Fabrication Processes of SiC MOSFETs

2-1 Design of edge termination structure

Under high voltage bias conditions, the high electric field is easily generated in the device and concentrates at the edge of the device. Therefore, edge termination techniques to decrease the electric field lower than the breakdown field of 4H-SiC are important. When there is no edge termination structure, the device is broken down under a low reverse voltage due to the local electric field concentration around the edge region. In previous reports, various edge termination techniques have been proposed [(2),(3)]. Additionally, we applied the field limiting rings (FLRs) to improve the blocking voltage.

Figure 1 shows the schematic cross-sectional structure of a 1,200 V MOSFET around the outer region of the device with both an active device cell as the transistor and the edge termination. The FLRs are p-type semiconductors that are indicated as p^- in the figure and are formed by ion implantation. We calculated the electric field in the MOSFET at 1,200 V bias by the device simulator "Atlas of Silvaco". The simulated electric field of the domain A-A' is shown by grayscale image in **Fig. 2**. **Figure 2 (a)** shows a simulated electric field without FLRs. The electric field is locally dense at the edge of the active device cell region and the maximum elec-

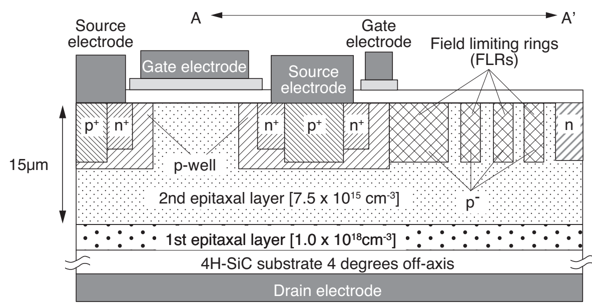

Fig. 1. Structure of 1,200 V MOSFET

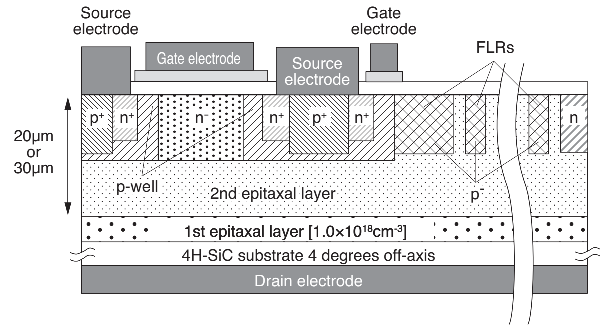

Fig. 3. Structure of 2,200V and 3,300V MOSFETs

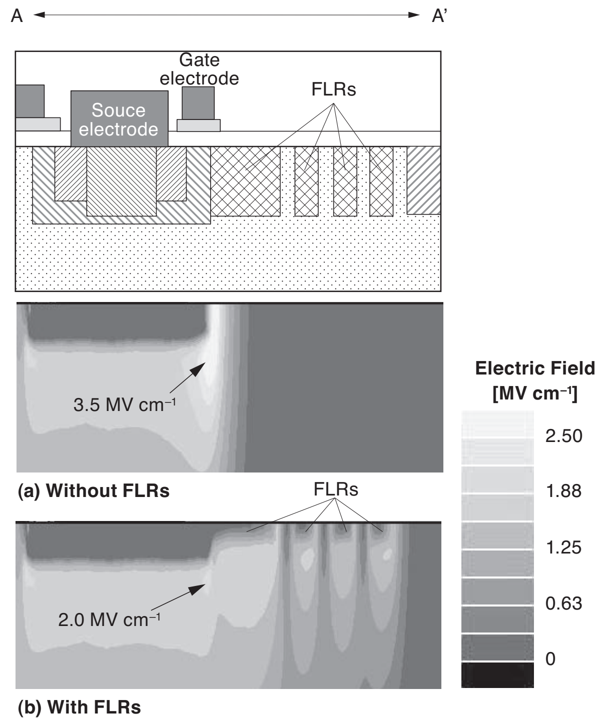

Fig. 2. Effect of FLRs on electric field

Table 1. Doping concentration of MOSFET

Part of implantation	Dose of implantation [cm^{-2}]
p^+	3.3×10^{15}
p-well	2.9×10^{13}
p^-	1.3×10^{13}
n^+	6.9×10^{14}
n	1.0×10^{13}
n^-	1.0×10^{11}

tric field in SiC is 3.5 MV cm^{-1}, which is greater than the critical breakdown field of 4H-SiC, 2.5 $MVcm^{-1}$. In the case of MOSFET with FLRs (**Fig.2 (b)**), the simulated electric field in SiC migrates toward the outer regions and the maximum is 2.0 MV cm^{-1}, which is lower than the critical breakdown field of 4H-SiC. We designed FLRs for the 2,200 V and the 3,300 V SiC MOSFETs in the same way.

2-2 Design and fabrication processes

Figure 3 shows the schematic cross-sectional structure of the 2,200 V and 3,300 V MOSFETs. The epitaxial layer was grown on an n-types 4H-SiC (0001) substrate. The doping concentration and the thickness of the epitaxial layer were 4.5 x 10^{15} cm^{-3} and 20 μm for a 2,200 V MOSFET, 3.0 x 10^{15} cm^{-3} and 30 μm for a 3,300 V MOSFET, respectively. The n^+ regions are formed by P ion implantation and the p^+, p-well, and FLRs are formed by Al ion implantation. **Table 1** shows a typical dose of each implantation. The channel length is 1 μm. The thickness of the gate oxide is 50 nm. The gate electrode is n-type polycrystalline silicon. In order to reduce the specific on-resistance, the ion implantation into the JFET region is also applied.

Figure 4 shows the fabrication process of an SiC MOSFET in detail.

(a) Epitaxial growth
The n-type 4H-SiC epitaxial layer is grown on 4 degrees off-axis (0001) substrate using chemical vapor deposition (CVD).

(b) Ion implantation
After the formation of SiO_2 mask, the n-type and p-type regions are formed by P and Al ion implantation, respectively. To prevent crystal defect of the epitaxial layer during the ion implantation, the wafer is heated to several hundred degrees Celsius.

(c) Activation annealing
To activate electrically implanted dopants electrically, and recover crystal defect caused by ion implantation, the wafer is annealed at high temperature.

(d) Gate oxidation
The gate oxide layer with a thickness of 50 nm is formed on the surface by dry oxidation, followed by nitridation.

(e) Formation of gate electrode
Polycrystalline silicon is formed on the gate oxide, using low-pressure CVD as a gate electrode. In order to increase electrical conductivity of the polycrystalline silicon, phosphorous diffusion is employed. Then, the unnecessary part of polycrystalline silicon is removed by dry etching.

(f) Formation of ohmic contact
First, the interlayer dielectric (SiO_2) is formed. Then,

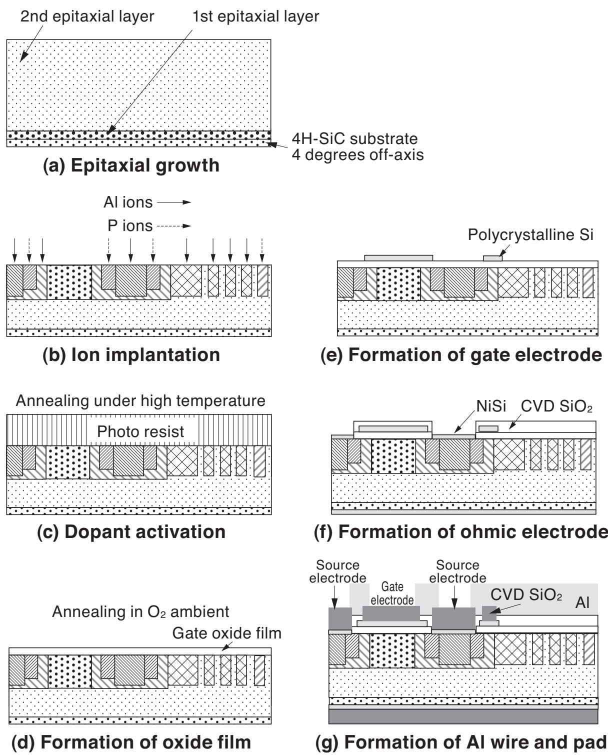

Fig. 4. Fabrication process of MOSFET

the SiO_2 is etched by dry etching to form the source contact hole, and the NiSi is deposited at the source contact region. The backside drain electrode is also formed by metal deposition. After that, the wafer is annealed to form the ohmic contact.

(g) Formations of source pad and gate wire

After the contact holes for the source and gate electrode are formed, the Al electrode layer is deposited by sputtering and isolated electrically to each other. SiO_2 passivation of 2 μm thick is deposited. After that, gate and source pads are exposed by RIE for wire bonding.

2-3 Packaging for device characterization

After the completion of the on-wafer process, screening is carried out by electrical characteristics measurement; the MOSFETs are mounted in TO-220 packages made of CuW in order to measure the electrical properties.

(a) Dicing

The fabricated wafer is cut into unit chips using a dicer.

(b) Mounting

A chip is mounted on a TO-220 package and attached by soldering.

(c) Wire bonding

Each electrode in the chip are electrically connected to the package terminal using Al wire.

(d) Plastic molding

To protect the device and provide isolation between Au wires, silicone gel is inserted until the wires are sealed completely.

3. Characteristics of MOSFET

3-1 Specific on-resistance of SiC MOSFET

Figure 5 shows the I_{DS}-V_{DS} characteristics of 2,200 V and 3,300 V MOSFETs and the specific on-resistance (V_{GS} = 15 V, V_{DS} = 2 V) are 12.6 mΩ cm^2 and 14.2 mΩ cm^2 at room temperature, respectively. Although the specific on-resistance of 3,300 V MOSFET is higher than that of the 2,200 V, this is because of the differences in the thickness and the doping concentration of the epitaxial layer.

3.2 Blocking characteristics of SiC MOSFET

Blocking characteristics of 2,200 V and 3,300 V MOSFET are shown in **Fig. 6**. The blocking voltage is defined at a drain leakage current of 1μA. The blocking voltage of 2,200 V and 3,300 V MOSFETs are 2,750 V and 3,850 V, respectively. These experimental blocking voltages are about 90-95% of the approximate parallel-plane blocking voltage estimated from the epitaxial layer and doping concentration.

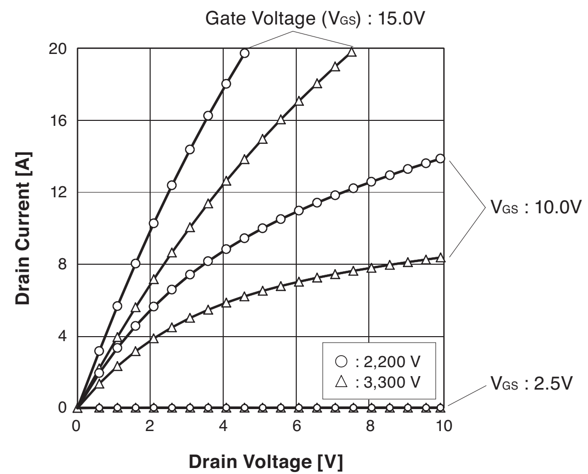

Fig. 5. I_{DS}-V_{DS} characteristics of 2,200 V and 3,300 V class MOSFETs

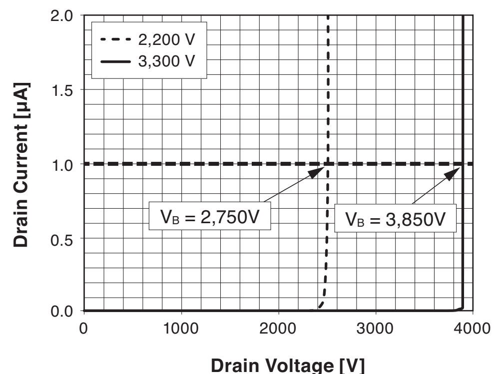

Fig. 6. Blocking characteristics of 2,200 V and 3,300 V MOSFETs

4. Prospects

In order to reduce the specific on-resistance, the ion implantation into the JFET region was also employed, and low specific on-resistance of 12.6 mΩ cm^2 and 14.2 mΩ cm^2 were obtained for the 2,200 V and 3,300 V SiC MOSFETs, respectively. These results show that the SiC MOSFETs are superior to the Si-IGBT in terms of the low specific on-resistance. Therefore, the SiC MOSFETs can contribute in reducing power loss in the power systems.

5. Conclusion

The authors developed a high blocking voltage MOSFET with FLRs using 4H-SiC, which is expected as a material that exceeds the performance limit of Si power devices.

The measured blocking voltage for 2.2 kV or 3.3 kV MOSFETs were 2,750 V and 3,850 V respectively, which correspond approximately to 90-95% of the parallel-plane breakdown voltage assumed from the thickness and doping concentration of the epitaxial layer. Implanted doping into JFET region was effective in reducing specific on-resistance, resulting in 12.6 mΩ cm^2 for 2.2 kV and 14.2 mΩ cm^2 for 3.3 kV MOSFETs at room temperature. These results indicate that SiC MOSFETs are applicable in high voltage converters and inverters. In order to improve SiC MOSFETs with higher blocking voltage, it is important to design edge termination structure in detail.

References

(1) M. Bhatnagar and B. J. Baliga, IEEE Transactions on Electron Devices, vol.40, pp.645-655, 1993.

(2) K. P. Schoen, J. M. Woodall, J. A. Cooper Jr., M. R. Melloch, IEEE Transactions Electron Devices, vol.45, pp.1595-1604, 1998.

(3) B. J. Baliga, Power semiconductor devices, Boston: PWS Publishing Co., 1995.

Contributors (The lead author is indicated by an asterisk (*).)

R. KIMURA*
• Power Device Development Division

K. UCHIDA
• Power Device Development Division

T. HIYOSHI
• Power Device Development Division

M. SAKAI
• Assistant Manager, Power Device Development Division

K. WADA
• Assistant Manager, Power Device Development Division

Y. MIKAMURA
• General Manager, Power Device Development Division