Material Characterization of Semiconductor Devices

Akira YAMAGUCHI

Analytical characterization techniques using a transmission electron microscope (TEM) or a focused ion beam (FIB) system have contributed to the development of semiconductor devices. In particular, at Sumitomo Electric, these techniques have been applied to the analysis of metal-InP interfaces and the investigation of ohmic contact formation mechanisms, with the aim of developing Pd based ohmic contacts for p-type InP which has a shallow reaction layer and low contact resistance. For the further reliability and quality improvement of semiconductor products, the author also conducted the development of TEM specimen preparation techniques by using FIB and sampling techniques. As a result, the degradation mechanism of GaAs transistors under high temperature operation and the electrostatic damage (ESD) induced degradation mechanism of InGaAsP LDs were clarified. This paper describes his study on the material development and reliability improvement for semiconductor devices by using characterization techniques.

Keywords: GaAs, InP, ohmic contacts, FET, LD, PD, ESD, TEM, FIB

1. Introduction

The full-scale progression of optical communications was triggered by the indication in 1966 of the possibility of using low-loss optical fibers for communications. Since then, optical communication technologies have advanced by the development of optical semiconductors such as the laser diode (LD) and photodiode (PD), along with high-speed semiconductor circuit technologies, including the laser driving circuits and integrated circuits for transmission signals; optical fibers used in the development of such technologies have losses of 0.2 dB/km or lower. This has allowed even residential users access to high-speed optical transmission lines as fast as 1 Gbps. The low-loss wavelength band of an optical fiber is in the 1.3 to 1.6 μm band, and InP materials are used for compound semiconductors that are compatible with this range of wavelengths. Since around 1980, light emitting diodes (LEDs), PDs, and LDs have been developed using InP semiconductors. By using the compound semiconductor wafers that have been developed since 1961, such as GaAs and InP, we launched the development of semiconductor devices in the late 1970s, which led to the development of systems and devices for the optical communication industry [(1)]. The development of these semiconductor devices required analytical characterization techniques, for instance, to verify the behavior of the added impurity and the composition and structure of the devices so as to improve the design of the manufacturing process. However, the analysis technology during the 1980s was not satisfactory for the measurement of the active layers that were micrometers to nanometers in thickness and micrometers in width. This necessitated the development of more sophisticated and accurate analysis technologies to solve problems related to device characteristics and reliability. This paper reports on the development of materials for semiconductor devices, as well as reliable technologies that are based on the latest developments in the field of material analyses.

2. Development of Ohmic Contact for P-type InP

2-1 What is an ohmic contact?

On the basis of the physical and electric behavior of electrons and holes inside a semiconductor, the semiconductor device communicates with an external circuit by passing an electric signal through electrodes attached to the semiconductor. Therefore, the electric current required to operate the device is applied to the semiconductor and the signal generated inside the semiconductor is transmitted to the external circuit through these electrodes. However, the contact between a metal and semiconductor results in a carrier shift at the contact interface because of the Fermi level alignment. As a consequence, a carrier deficiency occurs on the semiconductor surface and generates an energy barrier on the interface. As a result, diode-like rectification characteristics occur between the metal and semiconductor and extra potential is generated, interrupting the device operation. To achieve desirable characteristics between the semiconductor and metal electrodes, the free flow of electric current is required and the Ohm's law should be applicable; such a contact that follows the Ohm's law is called an ohmic contact.

An ohmic contact is an important part of a device because device characteristic cannot be achieved if the ohmic contact has poor characteristics, even if semiconductor crystalline quality and structures are excellent. The various devices that we have developed so far include GaAs LEDs, InP LEDs, GaAs transistors, InP PDs, InP LDs, ZnSe LEDs, GaN LDs, and SiC transistors; the development of all these devices required substantial amounts of time for the development of ohmic contact with repeated improvements. This paper mainly focuses on the development of ohmic contact for p-type InP. For a general explanation of an ohmic contact for compound semiconductors, please refer to previous literature [(2)].

2-2 Ohmic contact for p-type InP

The ohmic contact used for InP based optical and electronic devices, including optical communication InGaAs/InP PDs and InGaAsP/InP LDs, primarily requires

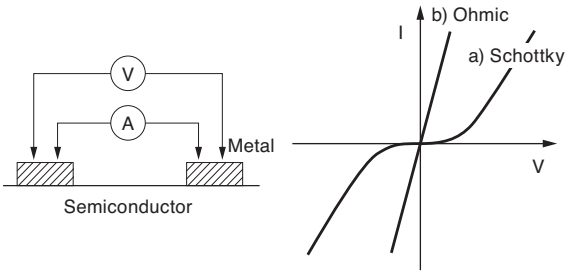

Fig. 1. Ohmic contact

a high reliability with a low contact resistivity, in addition to a method for low-cost manufacturing. The ohmic contact material for p-type InP generally employs AuZn and AuBe, which add the p-type impurities Zn and Be to Au as the base metal to achieve a lower contact resistivity below the 10^{-5} Ωcm^2 range. These contacts achieve a low contact resistivity by being annealed after deposition on the semiconductor surface by a reaction between the metal and semiconductor. However, they involve the following problems: (1) they are not suitable for thin-film devices because annealing process generates reaction layers thicker than 0.5 μm on the metal/InP interface, (2) they are not thermally stable, and (3) the annealing temperature reaches as high as 450°C, whereas that of the Au-GeNi material used as the n-type electrode in the device is only 400°C. **Photo 1** shows a cross-sectional micrograph of the AuZn ohmic contact obtained with scanning electron microscope (SEM). The figure reveals the generation of projecting reaction layers deeper than 0.5 μm on the metal/InP interface [3), (4)].

The mechanism of generating such deep reaction layers should be as follows. First, the AuZn deposited by the vacuum evaporation equipment forms a film after acid cleaning of the InP surface to expose a clean surface. However, as a native oxide film has already been generated on the InP surface by the time the vacuum evaporation equipment is introduced after acid cleaning, the deposited AuZn contact material cannot obtain direct contact with the semiconductor, and the interface presents the Schottky characteristic. Thus, the ohmic characteristic is achieved through annealing to obtain contact with the metal and semiconductor. Although the Au reacts well with the InP itself at 250°C or higher in this case, it diffuses into the InP for the first time at a temperature exceeding 400°C, as the material has a low reactivity to the native oxide film found on the interface. **Photo 2** shows a cross-sectional view of the native oxide film found on the InP surface with a transmission electron microscope (TEM). A specimen is prepared by evaporating Au as a protective layer to enable a cross-sectional observation of the native oxide film with an extremely thin surface. Enlarging the image by nearly a million times microscopically reveals that the film thickness varies depending on the position, and that a native oxide film between 1 and 4 nm thick covers the surface. The projecting reaction layers appear to have been generated due to the preferential reaction of the thin part of this native oxide film.

A close observation of how the AuZn contact is formed reveals that controlling the reactivity of the metal and the native oxide film is important and a key to obtaining a shallow reaction layer of even thickness.

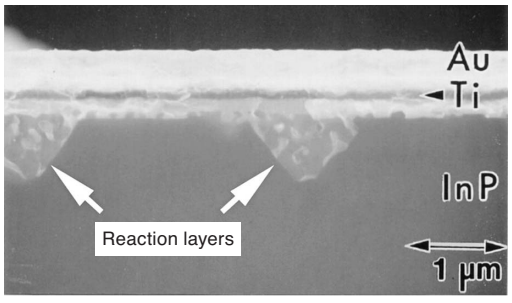

Photo 1. Cross-sectional SEM image of AuZn ohmic contact

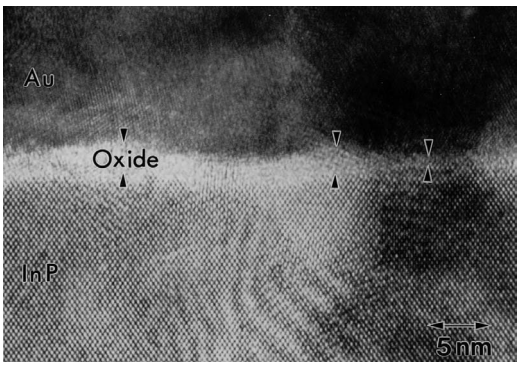

Photo 2. Native oxide film on InP surface

2-3 Near Noble Metals (Ni, Pd) Based Ohmic Contact

As mentioned above, although AuZn contacts achieve a low contact resistance, they generate thick reaction layers on the interface and need a relatively high annealing temperature. This shows the need for a new material that maintains the contact resistance in the 10^{-5} Ωcm^2 range, achieves shallow reaction layers at 0.1 μm or less, and lowers the annealing temperature to 400°C or lower. To achieve such an ohmic contact, it is important to find a method to control the native oxide film found on the interface between the metal and the semiconductor. Some effective methods might be: (1) a metal that has high reactivity with the native oxide film should be used; (2) the generation of the native oxide film should be prevented; or (3) such a film should be removed. The native oxide film may be removed by sputter cleaning the wafer surface inside the deposition equipment in addition to acid cleaning before evaporation; however, it is hard to apply this method to the p-type InP as sputtering results in donor-type defects on the surface [5)]. Further, the reported reduction effect on the native oxide film from creating an ultrathin film of Sb on the InP surface [6)] promises the removal of the native oxide film if Sb is used for the contact material. It is also known that the transition metals such as Ni and Pd, called near noble metals, have a high reactivity to the native oxide film of InP [7), (8)]. Although

there are some development examples of using these metals as the base metals for GaAs ohmic contacts [9], [10], their use with InP has not been sufficiently considered, requiring an investigation into what might be appropriate. Hence, research was conducted regarding an ohmic contact with a base of near noble metals such as Ni and Pd.

2-4 Interfacial reaction between near noble metals (Ni, Pd) and InP

To select an appropriate material for a new ohmic contact, it is primarily necessary to understand the reaction between the base metal and semiconductor, in other words, the type of interface reaction in annealing after the formation of a film of the contact material. Therefore, an annealed sample was prepared with a thin Ni or Pd film on an InP substrate, and the interfacial reaction products were investigated by both X-ray diffraction (XRD) and electron diffraction with the TEM, where the XRD fixed the angle of incidence at 5° to allow thin layers to be analyzed. **Table 1** lists the results of 2 min of annealing after the formation of a 50 nm layer of Ni or Pd on the InP substrate, presenting high reactivity, where both the Ni and Pd reacted with the InP at 250°C or below to generate ternary alloys, including $Ni_{2.7}InP$ and Pd_2InP. It was also revealed that in the case of Ni, the ternary alloy was decomposed to compounds such as Ni_2P and In once it exceeded 300°C, while in the case of Pd, the ternary alloy remained stable up to 450°C. It is necessary to understand how the generated compounds change in specific temperature ranges in order to select materials.

Table 1. Reaction products of Ni and Pd with InP

	Ni	Pd
250°C	$Ni_{2.7}InP$, Ni	Pd_2InP, Pd
300°C	$Ni_{2.7}InP$, Ni_2InP (Ni_2P)	Pd_2InP, (Pd)
400°C	Ni_2InP, Ni_2P, In ($Ni_{2.7}InP$)	Pd_2InP, (Pd_5InP)
450°C	Ni_2InP, Ni_2P, In	Pd_2InP, (Pd_5InP)
500°C	Ni_2InP, Ni_2P, In	PdIn, PdP_2

2-5 Effect of Zn addition

The standard method employed to achieve a favorable contact resistance in an ohmic contact is the addition of a p-type or n-type impurity to the base metal, for instance with AuZn, adding the secondary element Zn to the Au in the semiconductor. Therefore, a contact material with an M/Zn/M structure (where M stands for a metal, namely Ni or Pd, and a slash (/) represents the deposition sequence) was produced by adding Zn, a typical p-type impurity, to Ni and Pd. As a result, the contact resistance, which never fell to less than 1×10^{-4} Ωcm^2 with a single layer of Ni or Pd alone, became 4 to 7×10^{-5} Ωcm^2 through the addition of Zn. These contact materials had approximately 50 nm thick reaction layers with InP, which are suitable for the target of this study. We therefore achieved reaction layers of equal contact resistance that were one order shallower than AuZn.

It is believed that the contact resistance is lowered by the addition of Zn because, in case of AuZn, the evaporated Zn in the thin film is diffused into the semiconductor to enhance the carrier concentration on the semiconductor surface, which consequently changes the energy barrier between the metal and semiconductor. Thus, research was conducted to determine whether such a phenomenon occurred in this case as well. Electrochemical C-V measurements and SIMS measurements revealed that the carrier concentration in the p-type InP used for the experiment was approximately 4×10^{18} cm^{-3} on the InP surface due to the doping of Zn to the inside of the epitaxial layer of the semiconductor, while the Zn concentration was 1×10^{19} cm^{-3}. The optimal annealing temperature of the Pd/Zn/Pd contact material is 375°C, and the solid solubility of Zn in InP at this particular temperature is around 1×10^{18}cm^{-3} [11], indicating that the Zn in the InP is already supersaturated. Therefore, annealing at 375°C is thought to gradually diffuse Zn out of the InP. The next experiment involved the use of backside SIMS to determine whether the evaporated Zn is diffused into the InP at 375°C. In this method, secondary ion mass spectroscopy (SIMS) was used to measure, from the back side of the substrate, the impurities near the InP surface of a specimen produced by evaporating and annealing the contact material. Measurement should be conducted from the back side since an SIMS measurement from the metal side, which contains a large amount of Zn, cannot determine the presence or absence of a trace of Zn in the InP. This experiment revealed that the Zn evaporated from the contact material was not diffused into the InP. This shows that the lowered contact resistance from the addition of Zn in the M/Zn/M contact material, compared to a single layer of a near noble metal, was not because Zn from the M/Zn/M was diffused into the InP to enhance the carrier concentration. Taking into consideration that Zn that is not activated as the p-type carrier already exists in the InP (6×10^{18} cm^{-3}), the Zn addition to the electrode material would presumably result in an effect that suppresses the external diffusion of Zn into the InP (i.e., cap effect).

Figure 2 shows the annealing time dependence of the contact resistance, comparing the annealing temperatures (300°C for Ni and 375°C for Pd) that achieve the minimum contact resistance [12].

While in the case of Ni/Zn/Ni, the contact resistance increases by approximately one order of magnitude when the optimal annealing time of one minute is extended by another 0.5 minute, Pd/Zn/Pd maintains a resistance in the 10^{-5} Ωcm^2 range for a relatively long period of time, between 1.5 to 3 minutes, showing that Pd is more thermally stable. The reason for this phenomenon will be explained in **Fig. 3** using the energy band diagrams of the interface between the InP and metal. First, by annealing the Ni at 300°C for 1 min (a) and the Pd at 375°C for 1.5 min (c), contact with the highly doped p-type area is stably formed and a low contact resistance is achieved by the cap effect of the Zn included in the chemical compounds such as the $Ni_{2.7}InP$ and Pd_2InP present on the semiconductor surface, according to the result of Section 2-4. In the case of Ni/Zn/Ni, however, when the annealing time

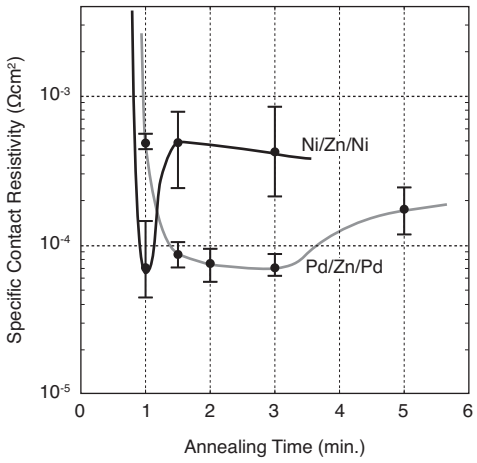

Fig. 2. Annealing time dependency of contact resistance

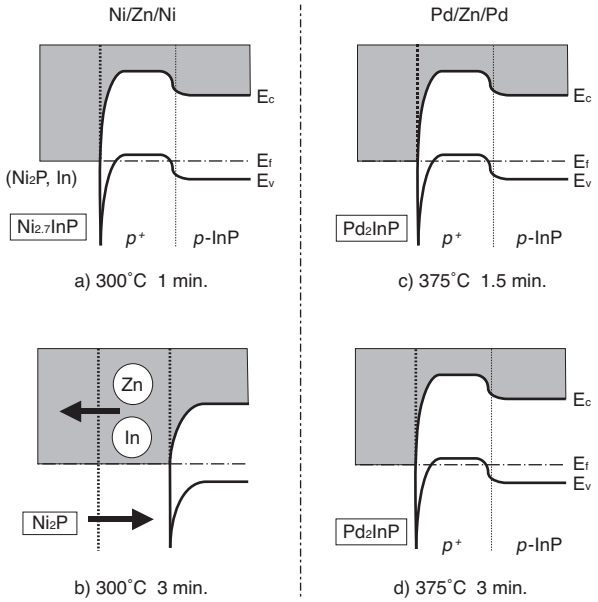

Fig. 3. Thermal stability of Ni/Zn/Ni and Pd/Zn/Pd contacts

is increased to 3 minutes, the $Ni_{2.7}InP$ of the interface starts decomposing into Ni_2P and In. This is because a temperature of 300°C, in the sense of a reaction between Ni and InP, is an intermediate transitional condition between 250°C or lower, where $Ni_{2.7}InP$ is stable, and 400°C or higher, where Ni_2InP, Ni_2P and In are stable. Once decomposition occurs, the Zn in the InP is diffused to the surface to lower the carrier concentration of the InP surface, increasing the contact resistance. In contrast, the Pd/Zn/Pd contact material might be more stable even for a longer annealing time, because the temperature of 375°C used to achieve the minimum contact resistance stays within the temperature range for the stable existence of the Pd_2InP generated through the reaction of Pd and InP. A comparison of Ni and Pd as the base metal for an ohmic contact for p-type InP shows that both can achieve reaction layers with a thickness of around 50 nm, as well as a contact resistance that is typically 7×10^{-5} Ωcm^2 or equivalent, but that the difference in the alloying reaction between the base metals and InP produces a difference in thermal stability, showing that Pd is more stable and therefore more preferable.

2-6 Problems with Pd/Zn/Pd ohmic contact

The abovementioned Pd/Zn/Pd structure is an excellent material that overcomes the problems with AuZn, but it was also revealed that shallow reaction layers resulted in negative effects, including extreme sensitivity to the condition of the InP surface and poor reproducibility. This would be problematic in product application. The application of acid cleaning to the InP surface immediately before evaporating the Pd/Zn/Pd contact material is insufficient to adequately remove surface contamination or native oxide films, possibly causing variations. Combining its use with physical etching such as ion sputtering may be possible, but creates the problem of damaging the InP surface.

Therefore, the introduction of Sb as a tertiary element was considered to solve this problem. The results obtained revealed that applying Sb on the InP surface reduces the native oxide film of the InP for AuZn contact materials and helps reduce the annealing temperature [13]. Therefore, an ultrathin (3 nm) Sb layer was adopted for the first layer of a PdZn-type ohmic contact. **Figure 4** shows the graph of the frequency against the contact resistivity after repeated experiments to compare the Pd (3nm)/Zn/Pd structure using Pd for the first layer with the Sb (3nm)/Zn/Pd structure using Sb for the first layer. It was revealed that the use of Sb for the first layer could stably maintain a lower contact resistance [14].

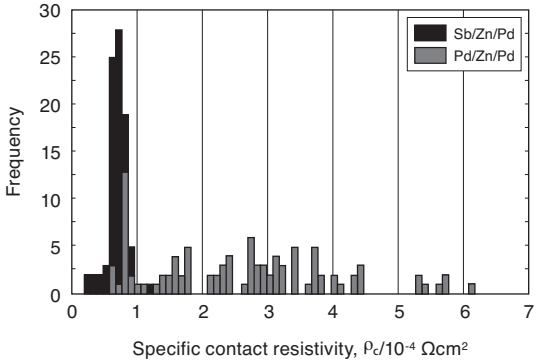

Fig. 4. Sb addition effect

The next experiment was a TEM observation of the interface to analyze the effect of the Sb addition. **Photo 3** shows the result of the cross-sectional TEM observation after evaporation but before the annealing of the Sb(3nm)/Zn(20nm)/Pd(10nm) structure. The observation found particles as large as approximately 30 nm on

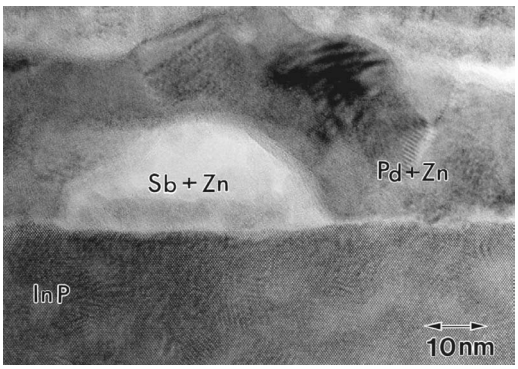

Photo 3. TEM image of Sb/Zn/Pd contacts (as deposited)

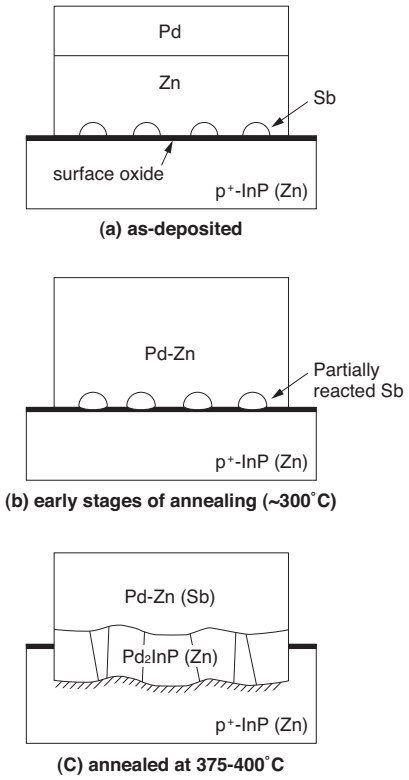

Fig. 5. Formation mechanism of Sb/Zn/Pd ohmic contacts

the InP. Energy dispersive X-ray analysis (EDX) revealed that the particle consisted of Sb and Zn. The island accumulation of evaporated Sb also found in the high resolution SEM observation of the surface would be the consequence of Zn adhering to the Sb and accumulating like an island. Further, the observation revealed that the area with no island also had Zn, which adhered to the InP surface. This Zn addition to the Pd/Zn/Pd contact material, which would help suppress the external diffusion of Zn in the InP as mentioned above, might have accelerated the suppressive effect of the external diffusion of Zn in the InP through the Zn directly attached on the InP surface by the Sb island. In other words, the Sb addition would not only reduce and remove the oxide film on the InP surface through the reduction effect, but also encourage diffusion control of the Zn in the InP by the attached Zn (**Fig. 5**).

2-7 Thermal stability of Sb/Zn/Pd ohmic contact

The application of the Sb/Zn/Pd contact material to semiconductor device products requires lowered wiring resistance and the preferable wire bonding characteristics. Therefore, a thick Au layer would have to be formed as the topmost layer of the contact materials. However, the direct formation of Au on the Sb/Zn/Pd may deteriorate the characteristics through inter-diffusion during annealing, therefore requiring a diffusion barrier layer (barrier material). The refractory metal Mo was found to be effective for this barrier material, and was used to form an Sb/Zn/Pd/Mo/Au structure.

The thermal stability of the completed structure was assessed since this dominates the reliability of any device produced. This assessment observed changes in the contact resistance after leaving the structure at a temperature as high as 300°C. Similar assessments were conducted with the AuZn contact material for comparison. **Figure 6** shows the results. The assessment revealed that the contact resistance of the AuZn contact material, of which the initial value was likely to be lower, sharply rose as the annealing time increased, finally reaching 10^{-4} Ωcm² after 2 h. In contrast, the contact resistance of the Sb/Zn/Pd/Mo/Au contact material was slightly high but stable and remained in the 10^{-5} Ωcm² range up to an annealing time of 3 h, confirming high reliability.

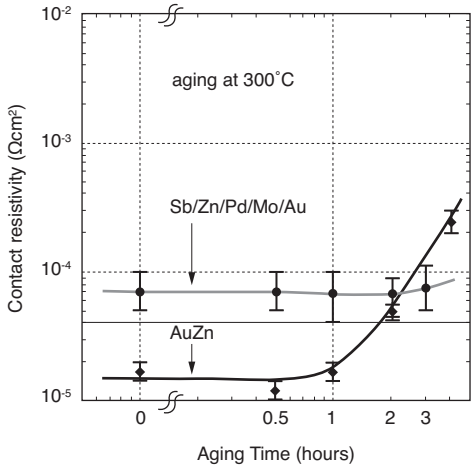

Fig. 6. Thermal stability of Sb/Zn/Pd/MoAu electrode

2-8 Summary

Although widely used for the contact material for p-type InP, an AuZn contact has problems, including reaction layers thicker than 0.5 μm, poor thermal stability, and a high annealing temperature of 450°C. Therefore, a contact material with a Pd base was developed to solve these

problems, and an Sb/Zn/Pd contact material with heat stability and reaction layers thinner than 0.1 µm was developed. The annealing temperature is feasible at 375 to 400°C, which is lower than the conventional AuZn and equivalent to AuGeNi, the standard material for the n-type InP ohmic contact. Considering the result, a reduction in the process cost can also be expected by simultaneously annealing the p-type and n-type ohmic contacts.

3. Degradation Analysis of Semiconductor Devices

3-1 Necessity of degradation analysis about practical devices for field use

The previous chapter reported on the development of novel ohmic contacts by making use of various material analysis techniques, including XRD, TEM, and SIMS. The development of such new materials does not involve the experimental production of a practical device at the primary stage of development but is more likely to focus on the production and analysis of test samples to measure just the characteristics being examined. Therefore, by producing a simple structure to measure a contact resistance and using such a simple test sample to form a film of the contact material on an epiwafer, it is possible during the development of ohmic contacts to compare the contact resistance or other characteristics with the materials or structures and then reflect the results in the device development. The development results are validated by producing a trial device and evaluating the device characteristics at a later stage of development. The use of a monitor sample suitable for the material analysis may be an indirect way of ascertaining the correspondence to the product characteristics but can still be used to produce various types of information through the execution of a variety of analysis methods. Thus, an adequate analysis of the characteristic formation mechanism is essential to understanding the nature of materials.

However, the shift to device production after the material development may cause an unexpected situation concerning its quality or problems threatening its reliability in the manufacturing process. In this case, the actual degraded devices must be analyzed individually. However, in this case, the analysis method is often restricted, and the methods that were performed in the previous chapter cannot be utilized sufficiently. For instance, an LD is as large as a 0.3 mm square, in addition to an operation layer with an area of around 1 × 300 µm, making it difficult to prepare a specimen for the TEM analysis, which is supposed to be a powerful analysis tool for a semiconductor device and yet is hardly applicable in this case. Hence, an analysis method enabling analyses of the practical product has been under development. In developing a method for preparing a specimen to allow the TEM to be applied to an analysis of the practical product, this paper reports the result of the application of such a method to a practical degradation analysis of a GaAs transistor and GaInAsP/InP LD.

3-2 TEM specimen preparation technique using focused ion beams

The TEM is an essential and important technique for semiconductor device analyses, and was used in analyzing the ohmic contacts of the previous chapter. By enabling atomic-level structural observation, as well as compositional and crystal-structural analyses through nm-beams as small as 1 nmø, the TEM can obtain some important information on the material phenomena that dominate device characteristics. Semiconductor device observations using the TEM have been conducted for Si integrated circuits (ICs) since around 1980. Cross-sectional observations started to be conducted with a TEM specimen produced by mechanically polishing a protective plate such as glass attached to the surface of an Si-IC chip to laminate it in the cross-sectional direction. Such cross-sectional observations allow the device process engineer who designed the process technique to directly compare the cross-section with the design. Therefore, these can be regarded as extremely important information. However, the TEM never came to be used for product degradation analysis or quality control despite being used for research and development because of the difficulty of preparing a TEM specimen, since the spot to be observed needed to be laminated thinner than 0.1 µm. **Figure 7** shows a conventional method for preparing a TEM specimen for cross-sectional observation. Such a specimen is prepared by cutting out a 2 to 3 mm chip and mechanically polishing the chip to laminate it, which makes it difficult to apply to a practical device where the operation layer is formed at the µm level.

In comparison, the preparation of a TEM specimen for a specific area of an Si device started to be attempted with the focused ion beam (FIB) used for repairing an IC, or for other purposes [15], around 1990 [16], [17]. An FIB is

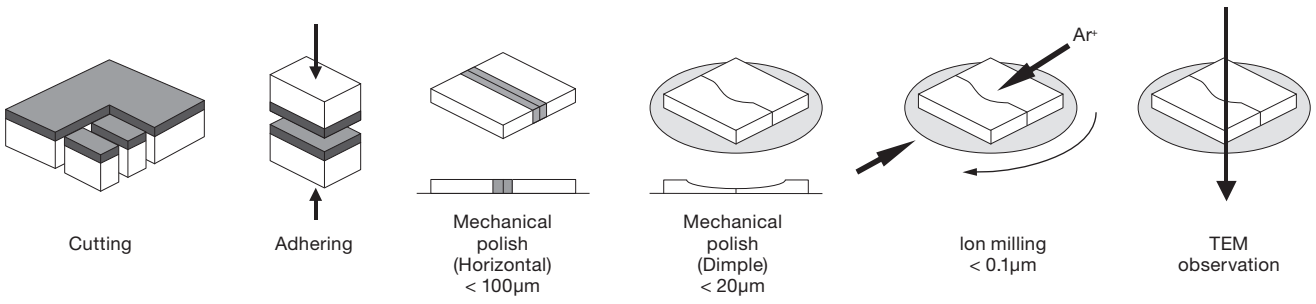

Fig. 7. Method to prepare specimen for cross-sectional TEM observation

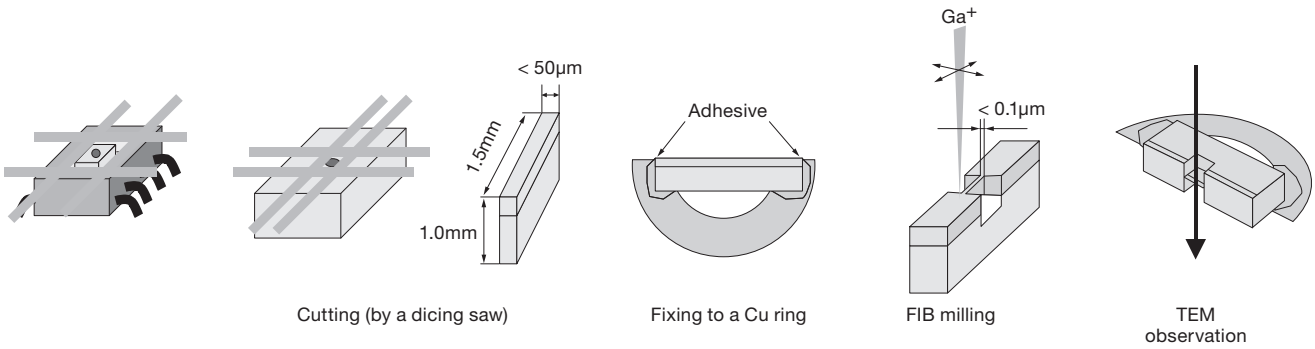

Fig. 8. Method to prepare TEM specimen by FIB

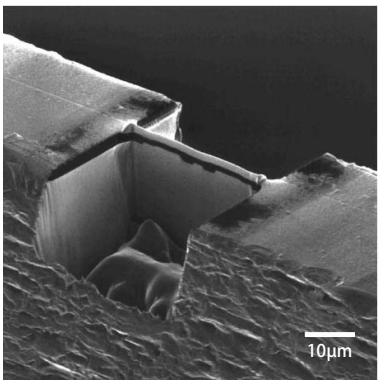

Photo 4. TEM specimen prepared by FIB

made by obtaining ionized Ga ions in an electrical field from the tip of a thin and sharp tungsten needle saturated with liquid metal Ga, accelerating them to tens of kilovolts and focusing to approximately 10 nmø. The beam is used for sputter-etching the object material like a scanning beam and observing an image similar to the scanning electron microscope (SEM), enabling the focused area of the device to be cut out with high resolution at the nm level. As one of the first companies to pay attention to this technique, we started the development to analyze the reliability of the GaAs IC electrode and the semiconductor interface under development at that time. With no example of an application to a compound semiconductor such as GaAs in those days, we developed the TEM observation of the device by considering the processing conditions suitable for GaAs, which is more significantly affected by the damage created by the ion beam processing than Si [18], and found a processing method that could reduce the damage to the more vulnerable InP [19]. **Figure 8** shows how a TEM specimen is prepared using the FIB. The TEM specimen is produced by the FIB by fixing a small chip cut out of the device by a dicing saw or other tool in advance on the TEM observation stage (Cu ring), and then making square holes of tens of micrometers at the right and left of the observed part, leaving a part as thin as 0.1 μm in the center. **Photo 4** shows a bird's eye view of the processed specimen. This method was applied to the newly developed high-speed GaAs transistor with the 0.18μm gate. Although a high temperature operation test verified high reliability where the mean time to failure (MTTF) was 240,000 h at 150°C, vertical and horizontal cross-sections of the gate electrode ('G' in the figure, composed of Ti/Pt/Au) in contact with the GaAs were cut out with the FIB to produce specimens for observation in order to analyze the failure mode in this case. **Figure 9** shows the result. The TEM observation and EDX analysis revealed that there were areas where Ti was diffused from the interface between the Ti and GaAs to the GaAs side, and that there was an occurrence of the gate-sinking phenomenon, in which Ti as the gate electrode metal sank into the GaAs [20]. Such a high-resolution observation and analysis of an electrode of a specific element in an IC can be achieved only by combining the FIB and TEM.

3-3 Innovation of TEM specimen preparation technique

The advancement of the TEM specimen preparation technique by the FIB processing promoted TEM observations of a device, which has been used to determine the cause of the degradation or failure of a real device. In the TEM sample preparation, however, the production process for the chip to place on the TEM stage (a Cu ring with a diameter of 2 to 3 mm) was a problem. The practical device analysis required multiple attempts to cut out a chip from a device, which was usually mounted in a metal or ceramic package, consequently taking a substantial amount of time. Further, this chip needed to be thinner than 50 μm (for instance 30 μm) because otherwise the FIB needed to form a large opening, which not only consumed time for the FIB processing but generated interference X-rays in the EDX analysis [21]. Therefore, this chip was cut out using a dicing saw as a highly accurate cutter, which required experience and skill, and still often resulted in failed attempts. Such a problem occurred when the practical device analysis needed to successfully observe only a single sample. This led to attempts to create a better sampling technique around 1998, where the part to be observed was directly cut out by the FIB with the device mounted in the package without any mechanical processing with a dicing saw or other tools [22], and we also started studying the creation of a simplified sampling system. **Figure 10** shows this method.

The invention of such a sampling method revolution-

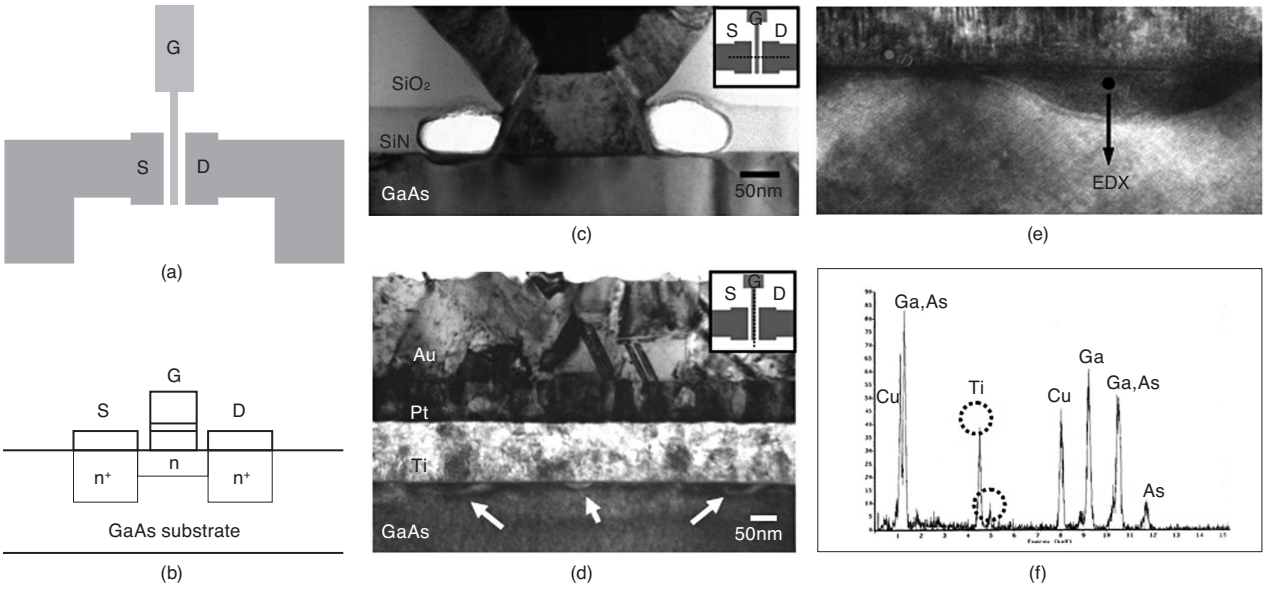

Fig. 9. Schematic diagram of GaAs transistor, (a)plan view, (b) cross-sectional view . (c) Vertical cross sectional TEM image of gate electrode, (d) Perpendicular cross sectional TEM image of gate electrode, (e) Enlarged view of figure d, (f) EDX spectrum of point A in figure e

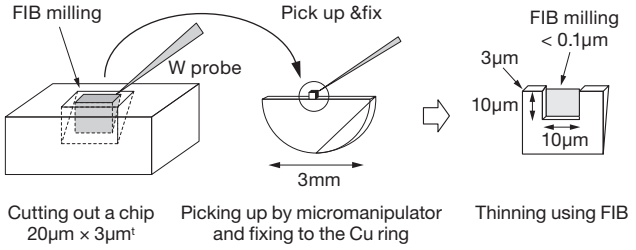

Fig. 10. Sampling method for TEM section

arily accelerated TEM specimen production using an FIB. It also improved the extraction accuracy of the part to be observed, in addition to the EDX analysis accuracy. This technique is now essential for TEM observations of a practical device, and the TEM technology is used, not only in research, but for a wide range of purposes, including reliability assessment.

3-4 Degradation analysis of GaInAsP/InP LD

Corresponding to the optical communication waveband, the GaInAsP/InP LD is widely used as the light source for optical communications, but requires high reliability. We have analyzed various degradation mechanisms associated with the reliability of the InGaAsP LD, to improve it by applying quality control technology. In this regard, this paper reports the improvement of LD chips by paying attention to the tolerance against electrostatic discharge (ESD), which is one of the important barometers of reliability [23] - [28].

One of the solutions against ESD may be an external electronic circuit that prevents the device from being destroyed by an external electrostatic discharge where the LD chip is mounted and an electronic circuit is incorporated as a module. However, this circuit is likely to be directly and electrically damaged by a human body, machine, or other factor in its handling in the implementation of the LD chip. Therefore, since the ESD tolerance of the LD chip itself should be improved, an analysis of the degradation mechanism by the ESD and the development of a degradation control technology have been conducted. The consideration to improve the ESD tolerance primarily requires an analysis of the degradation mechanism of the LD degraded in the ESD test.

Figure 11 shows the structure of the LD to be analyzed. This LD has a structure in which a 300 μm long InGaAsP active layer is buried in InP and trenches are formed at the right and left of the stripe.

An investigation of the degradation mechanism of the LD begins with estimating, using an LD characteristics analysis, whether the degraded point exists in the active layer itself, in the peripheral InP buried area, or in the electrode. If the active layer was degraded, the particular spot of the 300 μm long active layer stripe must be clarified. The analysis technique using the combination of the FIB and TEM, as mentioned in the previous section, may be available as a technique to observe and analyze the state of degradation, but is inefficient to thoroughly observe the 300 μm stripe. Here the observation of an electroluminescence image (EL image) of the active layer seems to be able to identify the degraded area through the change in the luminescence intensity [29]. For instance, if the degradation resulted from a crystal defect in the active layer, the EL intensity of such a failed area will be lowered. Therefore, viewing the EL image can identify a non-luminescent part. However, observation of an EL

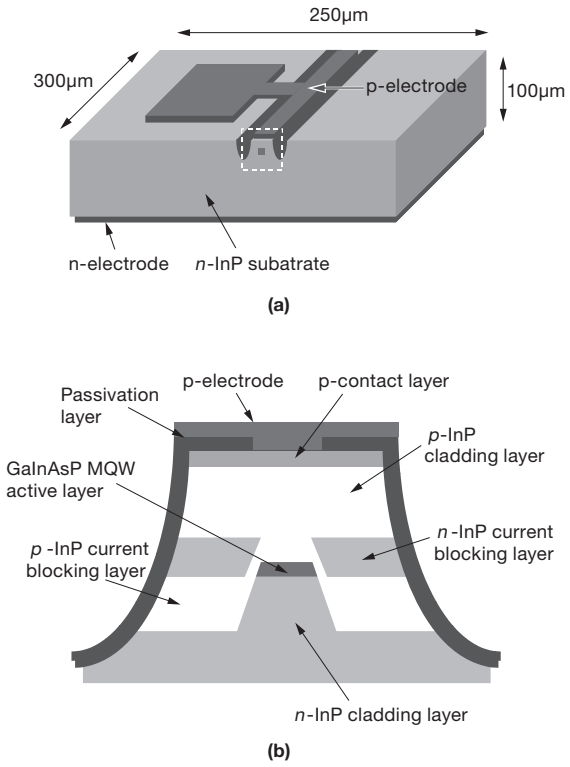

Fig. 11. Structure of InGaAsP/InP LD

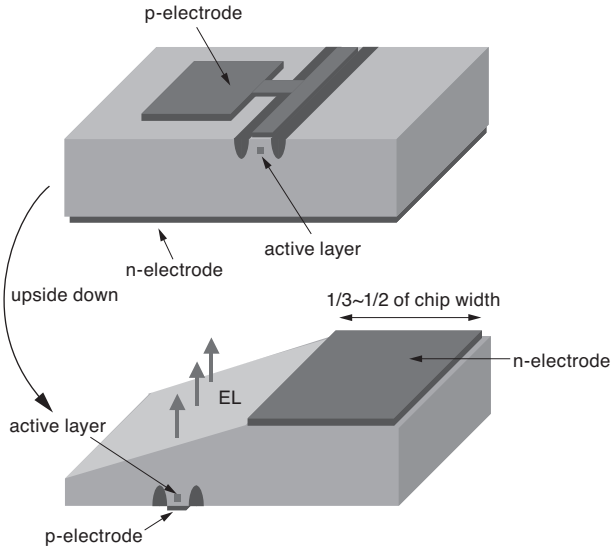

Fig. 12. Specimen for EL observation of InGaAsP/InP LD

image is difficult in a practical LD device, not only because an active layer is buried into the InP, but because it is blocked by the electrode formed on the chip surface. To solve this problem, a method for observing an EL image from the back of the polished chip was developed, as shown in **Fig. 12**. In this method, the chip was processed to enable observation of the luminance of the active layer stripe from the back of the chip through the InP substrate (the InP is transparent to the luminescence wavelength) by removing the LD chip mounted to the package to polish the back of the LD slantwise. After mounting this specimen again to the package back side up, the chip was energized to observe the luminescence from the active layer using an infrared microscope.

Photo 5 shows an example of the observation results of the degraded LD in an ESD tolerance test using this method. A non-luminescent area is seen close to the back facet of the LD, indicating that there may be an abnormality in the active layer in that position. Next, **Fig. 13** shows the observation result for a TEM specimen of this non-luminescent area produced through the sampling technique discussed in the previous section. This is a result of repeated operations with a large current pulse (application by a typical human body model) in the forward direction of the LD in the ESD tolerance test. It was revealed that in the LD chip, the fault progressed from the back facet into the internal direction as the pulse operation proceeded.

The failure mechanism in which crystal defect begins from the back facet in the ESD tolerance test is similar to the catastrophic optical damage (COD) reported in the AlGaAs high-power LD in the sense that the output light is absorbed via the non-luminescent recombination level of the crystal back facet of the LD and rapid heating melts the back facet, resulting in laser destruction. The optimization of the pre-forming processing of a coating film on the LD back facet formed to control the reflection ratio and prevent the degradation of the back facet could

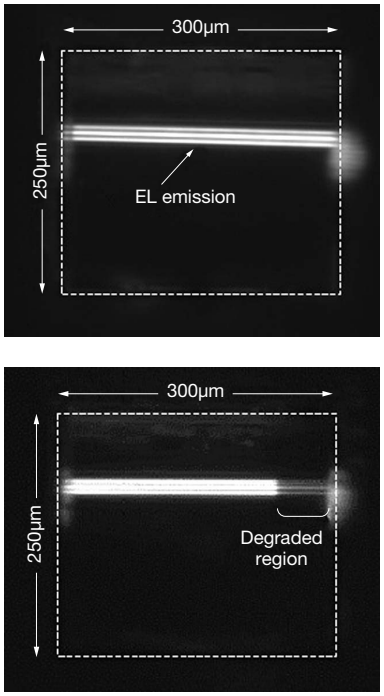

Photo 5. EL image of degraded LD in ESD tolerance test

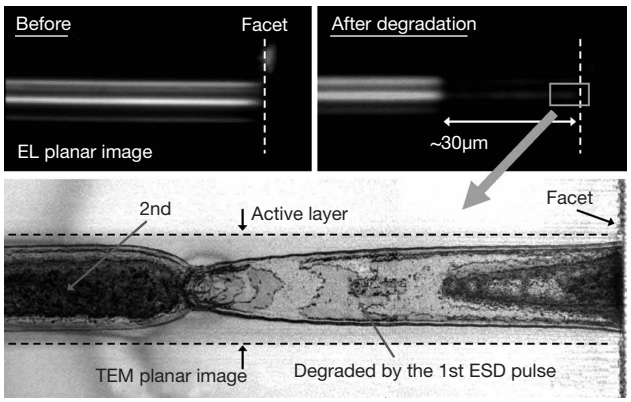

Fig. 13. TEM planar image of active layer of degraded LD in ESD test

significantly improve the ESD tolerance.

3-5 Summary

A TEM is an essential tool for material analyses of semiconductor devices, enabling structural observations at the atomic level of resolution and analyses at nm-resolutions. However, the difficulty of preparing an observation specimen has hindered the analysis of practical devices, making it difficult to adequately apply the tool to reliability or quality control. However, the practical application of the direct sampling technique using a focused ion beam or the mounting device as a technique to produce an observation specimen has been able to enhance device analysis to a practical level. This method revealed the failure mode in the reliability test for a high-speed GaAs transistor, and the degradation mechanism for an InGaAsP LD was analyzed in an ESD tolerance test to apply degradation control technology to the product. The highly reliable technology of the device was established by making use of such material analysis technology to promote device production, achieving the shipment of 10 million optical communication devices in January 2007.

4. Conclusion

The development of the GaAs integrated circuits, InP photodiodes, and optical devices including laser diodes that have been well underway since the mid 1980s have utilized analytical characterization technologies such as the transmission electron microscopy, X-ray diffraction, and secondary ion mass spectroscopy. The analytical technique that was available at the beginning of these developments did not necessarily satisfy the device analysis needs. Because of this, device analyses were carried out simultaneously with the development of the analysis technology itself. The development of an ohmic contact material was carried out using test samples, which enabled a detailed analysis despite its relatively indirect relation with the characteristics of the practical device, and therefore could fully reveal the formation mechanism of the characteristics. The solution to the problems regarding the establishment of product reliability and quality control, which essentially requires the analysis of a practical device, involves the development and application of a specimen production method that makes use of a focused ion beam in order to apply transmission electron microscopy as the most intensive analysis technology. Consequently, this technology not only considerably contributed to product commercialization by solving the problems associated with device reliability but also established the transmission electron microscope as more than just a tool to develop new products, making it a tool to evaluate reliability and achieve quality control.

Future issues that need to be analyzed include the development of novel analysis technologies and enhancements to the tools currently used to analyze practical devices. For instance, the former requires the use of a new beam such as synchrotron radiation, whereas the latter requires the practical use of technology that will enable the evaluation of the electric characteristics in a nanometer-sized area, such as scanning spreading resistance microscopy (SSRM) [30]. It is important to make use of these technologies to promote the development of both the analyses of device material physics and product analyses. Finally, the author expects that new devices currently under development will be commercialized as soon as possible to increase the volume of sales of these devices.

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Contributor

A. YAMAGUCHI

• Senior Specialist
Dr. Eng.,
General Manager, Core-technologies R&D Department, Semiconductor Technologies R&D Laboratories
He is engaged in the development of photonic devices using nitride semiconductors and the application research of compound semiconductors.